Abstract of the Disclosure

An embodiment of this invention pertains to a 3-sided routing architecture to interconnect function blocks, such as logic array blocks ("LABs"), within a programmable logic device ("PLD"). In the 3-sided routing architecture, inputs and outputs on a first side of a function block connect to a first channel, and inputs and outputs on a second side of the function block connect to a second channel where the second side is opposite the first side. Inputs and outputs on a third side of the function block connect to a third channel. A fourth channel associated with a fourth side of the function block, the fourth side opposite the third side, is coupled only to the first channel and the second channel. In one configuration, the inputs and outputs on each of the first side, the second side, and the third side have an equal number of inputs and outputs. In this configuration, each of the first channel, the second channel, and the third channel have the same width. In another configuration, the number of pins on one of the first side, the second side, or the third side differs from the number of pins on another one of those sides. In this configuration, the width of one of the first channel, the second channel, or the third channel differs from the width of another one of those channels. Input multiplexers route signals from the wires of the channels to the inputs of the function block. Output multiplexers and drivers drive the outputs of the function block through the wires of the channels. By placing the input multiplexers and the output multiplexers in certain relative arrangements, the logical distance that an output signal from the function block can travel on a wire is increased and that signal can be looped back to itself. In addition, each of the inputs and the outputs of the function block can be connected to both horizontal and vertical channels, and an output of the function block can be directly connected to an input of an adjacent function block.